UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,168	10/22/2001	Nai-Shung Chang	JCLA6880	4878

7590 06/17/2004

J.C. Patents, Inc.
Suite 250
4 Venture
Irvine, CA 92618

EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	3

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/036,168	CHANG ET AL.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-17* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 6-8, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said second pins" in line 6 of page 12. There is insufficient antecedent basis for this limitation in the claim.

Claim 15 recites the limitation "said step of delaying" in line 11 of page 17. There is insufficient antecedent basis for this limitation in the claim.

Claims 6-8 include the limitation of "said fourth resistor has a resistance different from that of said fourth resistor (lines 18-19 of page 14). It is not clear how the fourth resistor has a resistance different from itself.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 and 9-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al. (5,761,479) (hereinafter Huang).

As to claim 1, Huang teaches an apparatus for supporting multi-processors (abstract), wherein said apparatus is coupled to a central processing unit (CPU) socket (e.g. socket 1001), having a plurality of connecting pins (e.g. pin B14, S10, A13, C14,...) (tables 2-3 and col. 20, lines 17-67), and when said CPU socket is inserted with a first type CPU, a first pin (e.g. B14) among said connecting pins has a first equivalent resistance, and when said CPU socket is inserted with a second type CPU, said first pin has a second equivalent resistance (col. 20, lines 25-28), said apparatus comprising: a distinguish device (identifying circuit), coupled to said first pin to apply a difference between said first and said second resistance to generate a CPU select signal (identification signal) (col. 22, lines 54-63); and a switch circuit (31 and associate circuitry), coupled to said distinguish device and said CPU socket to selectively connect a plurality of first type CPU signals to said corresponding connecting pins, and a plurality of second CPU signals to said corresponding connecting pins according to control of said CPU select signal (at least Fig. 10, and col. 20, lines 7-67).

As to claim 2, Huang further teaches said CPU socket is inserted with said first type CPU, a second pin (e.g. A13, C14, S10) among said connecting pins has a third equivalent resistance, and when said CPU socket is inserted with said second type CPU, said second pin has a fourth equivalent resistance (col. 20 lines 65-67, col. 21 lines 24-67), and said distinguish device is coupled to said second pin to use a difference between said first, second, third and said fourth equivalent resistance to determine a type of said

CPU inserted in said CPU socket, and to generate a CPU select signal (Figs. 10-11 and col. 22, lines 1-44).

As to claim 3, Huang further teaches said apparatus further receives a suspend status input signal (CPURST, BREQ), and said distinguish device further comprises: a processor select circuit (30 and associate circuitry) (Fig. 11), coupled to said first and said second pins to use a difference between said first, said second, said third and said fourth equivalent resistance to generate a CPU select signal; and an interval control circuit (2) (Fig. 3), to receive said suspend status input signal and delay said suspend status input signal with a predetermine stop determination time, so that said processor select circuit cuts off said connection between said first pin and said processor select circuit (col. 9 line 59 to col. 10 line 17).

As to claim 4, Huang further teaches said interval control circuit comprises: a first delay circuit (timing control logic means U7), receiving and delaying said suspend status input signal with said predetermined stop determination time to generate a cutoff activating signal (DP23*); and a second delay circuit (delay circuit U8), coupled to said first delay circuit to receive said cutoff activating signal and to generate a suspend status output signal (P9RST) after delaying a predetermined buffer time; wherein said interval control circuit enable said processor select circuit to cut off a connection between said processor select circuit and said first and second pins, and a computer system that comprises said apparatus outputs a signal to activate according to said suspend status output signal (Fig. 3 and col. 9 line 59 to col. 10 line 17).

As to claim 9, Huang further teaches receiving a suspend status input signal (CPURST, BREQ), wherein said distinguish device further comprises: a processor select circuit (30 and associate circuitry) (Fig. 11), coupled to said first pin to use a difference between said first equivalent resistance and said second equivalent resistance to generate said CPU select signal; and an interval control circuit (2) (Fig. 3), to receive and delay said suspend status input signal with a predetermined stop determination time, so that said processor select circuit cuts off a connection between said first pin and said processor select circuit (col. 9 line 59 to col. 10 line 17).

As to claim 10, Huang further teaches said interval control circuit comprising: a first delay circuit (timing control logic means U7), to receive and delay said suspend status input signal with a predetermined stop determination time to generate a cutoff activating signal (DP23*); and a second delay circuit (delay circuit U8), coupled to said first delay device to generate a suspend status output signal (P9RST) after receiving and delaying said cutoff activating signal with a predetermined buffer time; wherein said interval control circuit cuts off a connection between said first pin and said processor select circuit according to said cutoff activating signal, and a computer system comprising said apparatus is activated according to said suspend status output signal (Fig. 3 and col. 9 line 59 to col. 10 line 17).

As to claim 11, Huang further teaches the apparatus further coupled to a power regulator (10 and associate circuits 1, 11) that provides a correct source voltage to said CPU inserted in said CPU socket according to said suspend status output signal and said CPU select signal (col. 5, lines 33-67).

As to claim 12, Huang further teaches said processor select circuit comprises an activate determination control circuit that enable said processor select circuit to operate after receiving said suspend status input signal, so as to determine said type of said CPU inserted in said CPU socket (changing BOFF# from "0" to "1" to release '486 from HOLD and allow '486 g into normal operation) (col. 10, lines 9-17).

As to claim 13, Huang further teaches said distinguish device is supplied power from a prepared power supply (10) (col. 5, lines 33-67).

As to claim 14, Huang teaches a method for supporting multi-processors in a single motherboard, applied to a computer system (abstract) that comprises a CPU socket (e.g. socket 1001) and a suspend status input signal (CPURST, BREQ), wherein the CPU socket comprises a plurality of connecting pins (e.g. pin B14, S10, A13, C14,...) (tables 2-3 and col. 20, lines 17-67) of which a first pin (e.g. B14) has a first equivalent resistance when a first type CPU is inserted in said CPU socket, and has a second resistance when said CPU socket is inserted with a second type CPU (col. 20, lines 25-28), said method comprising: using a difference between said first equivalent resistance and said second equivalent resistance to generate a CPU select signal (identification signal) (col. 22, lines 54-63); and selectively connecting a plurality of first CPU signals to said corresponding connecting pins, and a plurality of second type CPU signals to said corresponding pins according to said CPU select signal (at least Fig. 10, and col. 20, lines 7-67).

As to claim 15, Huang further teaches delaying said suspend status input signal with a predetermined stop determination time after receiving (by timing control logic

means U7), and determining which type of said CPU is inserted in said CPU socket within said predetermined stop determination time (col. 9 line 59 to col. 10 line 17).

As to claim 16, Huang further teaches delaying the suspend status input signal with a predetermined buffer time (by delay circuit U8) after the predetermined stop determination time to allow said CPU is inserted in said CPU socket operating normally (col. 9 line 59 to col. 10 line 17).

As to claim 17, Huang further teaches a second pin (e.g. A13, C14, S10) among said connecting pins has a third equivalent resistance when said first type CPU is inserted in said CPU, and has a fourth equivalent resistance when said second type CPU is inserted in said CPU (col. 20 lines 65-67, col. 21 lines 24-67), and a difference between said third equivalent resistance and said fourth equivalent resistance is used to determined said type of said CPU inserted in said CPU socket (Figs. 10-11 and col. 22, lines 1-44).

Allowable Subject Matter

4. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 5 includes the limitation of a first resistor, with a first end coupled to a fixed voltage and a second end; and a latch circuit, with an input terminal, an output terminal and a control terminal, wherein said control terminal is coupled to said first delay device and said input terminal is coupled to said second end of said first resistor to receive a control of said cutoff

activating signal and outputs a cutoff latch signal, which is not shown by the prior art of record, in the combination as disclosed and claimed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses detecting the type of the CPU connected by sensing the pin state and providing proper voltage to the connected CPU:

US Patent	5,714,873	Hwang
US Patent	5,758,108	Nakamura
US Patent	6,381,693	Fish et al.
US Patent	5,931,930	Krick et al.
US Patent	5,884,091	Ghori et al.
US Patent	5,848,250	Smith et al.
US Patent	5,408,611	Kim
US Patent	6,327,663	Isaac et al.
US Patent	6,691,235	Garcia et al.
US Patent	5,819,050	Boehling et al.
JP Pat-No	JP405204844	Pan-Ratzlaff
European Patent Application	92116387.9	Yamaki et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha U. Vu
Examiner
Art Unit 2112

uv

SUMATI LEFKOWITZ
PRIMARY EXAMINER